

IN THE CLAIMS:

Please amend claims 1-5 as follows.

1. (Currently Amended) A variable dividing circuit comprising:  
  
a shift register configured by a cascade connection of D-type flip-flops ~~with an initializing means by clock synchronization,~~ wherein the D-type flip-flops respectively generate output signals; and  
  
a selecting ~~means for selecting~~ circuit which selects any one of the output signals at ~~respective stages of said shift register~~ as an output signal of the variable dividing circuit;  
  
wherein ~~said variable dividing circuit initializes each stage of said~~ the D-type flip=flops are respectively reset by the selected one of the output signals.
2. (Currently Amended) The variable dividing circuit according to claim 1,  
wherein an H level signal is inputted in a first stage of said D-type flip flop;  
~~said initializing means comprises a reset means;~~ and  
said selecting ~~means~~ circuit comprises a multiplexer.
3. (Currently Amended) The variable dividing circuit according to claim 1,  
wherein an H level signal is inputted in a first stage of said D-type flip-flop;  
~~said initializing means comprises a reset means;~~ and  
said selecting ~~means~~ circuit comprises a switch circuit.
4. (Currently Amended) The variable dividing circuit according to claim 1,  
wherein an L level signal is inputted in a first stage of said D-type flip flop;  
~~said initializing means comprises a preset means;~~ and  
said selecting ~~means~~ circuit comprises a multiplexer.

5. (Currently Amended) The variable dividing circuit according to claim 1,  
wherein an L level signal is inputted in a first stage of said D-type flip-flop;  
~~said initializing means comprises a present means;~~ and  
said selecting ~~means~~ circuit comprises a switch circuit.